EIGHT-BIT INPUT/OUTPUT PORT

DESCRIPTION

The μPB8212 input/output port consists of an 8-bit latch with three-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the control and generation of interrupts to the microprocessor.

The device is multimode in nature and can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

FEATURES

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current – 0.25 mA Max
- Three State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8080A Processor
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count
- Available in 24-pin Plastic and Cerdip Packages

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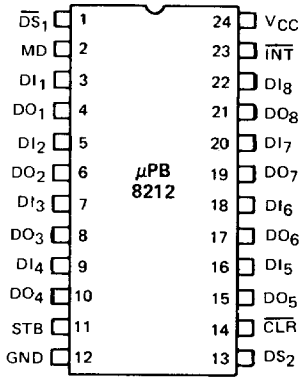
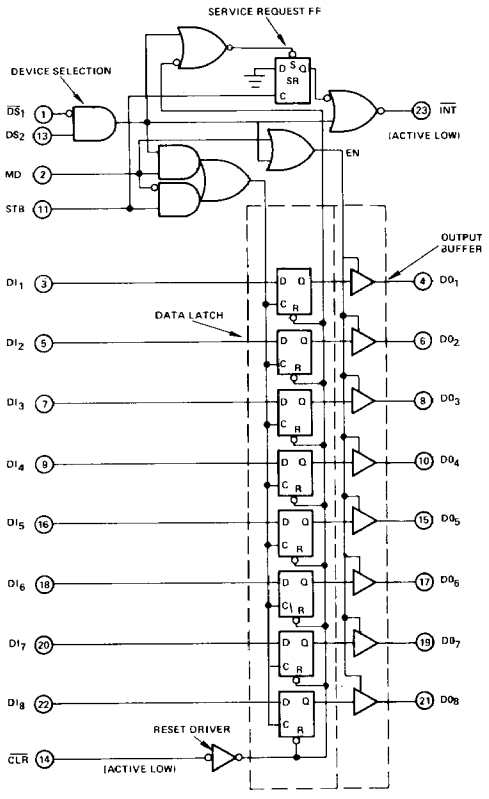
PIN CONFIGURATION



PIN NAMES

$DI_1 - DI_8$	Data In
$DO_1 - DO_8$	Data Out
$\overline{DS}_1$, DS_2	Device Select
MD	Mode
STB	Strobe
$\overline{INT}$	Interrupt (Active Low)
$\overline{CLR}$	Clear (Active Low)

BLOCK DIAGRAM



STB	MD	$(\overline{DS_1} \cdot DS_2)$	DATA OUT EQUALS
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

CLR	$(\overline{DS_1} \cdot DS_2)$	STB	SR ②	INT
0	0	0	1	1
0	1	0	1	0
1	0	0	③	③
1	↓	0	1	1
1	0	↓	0	0
1	1	0	1	0
1	1	↓	0	0

Notes: ① $\overline{CLR}$ resets data latch sets SR flip-flop. (No effect on output buffer)
② Internal SR flip-flop
③ Previous data remains

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	125 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current STB, DS_2, $\overline{CLR}$, $DI_1 - DI_8$ Inputs	I_{IL1}		−0.25	mA	V_F = 0.45V
Input Load Current MD Input	I_{IL2}		−0.75	mA	V_F = 0.45V
Input Load Current $\overline{DS_1}$ Input	I_{IL3}		−1.0	mA	V_F = 0.45V
Input Leakage Current STB DS, $\overline{CLR}$, $DI_1 - DI_8$ Inputs	I_{IH1}		10	μA	V_R = 5.25V
Input Leakage Current MD Input	I_{IH2}		30	μA	V_R = 5.25V
Input Leakage Current $\overline{DS_1}$ Input	I_{IH3}		40	μA	V_R = 5.25V
Input Forward Voltage Clamp	V_C		−1.0	V	I_C = −5 mA
Input "Low" Voltage	V_{IL}		0.85	V	
Input "High" Voltage	V_{IH}	2.0		V	
Output "Low" Voltage	V_{OL}		0.48	V	I_{OL} = 15 mA
Output "High" Voltage	V_{OH}	3.65		V	I_{OH} = −1 mA
Short Circuit Output Current	I_{O5}	−15	−75	mA	V_O = 0V V_{CC} = 5V
Output Leakage Current High Impedance State $DO_0 - DO_8$	I_O		20	μA	V_O = 0.45V/5.25V
Power Supply Current	I_{CC}		130	mA	

CAPACITANCE ①

T_a = 25°C; V_{CC} = +5V; V_{BIAS} = 2.5V; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		12	pF	$\overline{DS_1}$, MD
Input Capacitance	C_{IN}		9	pF	DS_2, $\overline{CLR}$, STB, $DI_1 - DI_8$
Output Capacitance	C_{OUT}		12	pF	$DO_1 - DO_8$

Note: ① This parameter is periodically sampled and not 100% tested

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Pulse Width	t_{pw}	30		ns	Input Pulse Amplitude = 2.5V
Data To Output Delay	t_{pd}		30	ns	
Write Enable To Output Delay	t_{we}		40	ns	Input Rise and Fall Times = 5 ns
Data Setup Time	t_{set}	15		ns	
Data Hold Time	t_h	20		ns	Between 1V and 2V
Reset to Output Delay	t_r		40	ns	Measurement made at 1.5V with 15 mA
Set To Output Delay	t_s		30	ns	
Output Enable/Disable Time	t_e/t_d		45	ns	① and 30 pF Test Load
Clear To Output Delay	t_c		55	ns	

Notes: ① R_1 = 300Ω/10KΩ; R_2 = 600Ω/1KΩ

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Data Latch

The 8 flip-flops that compose the data latch are of a "D" type design. The output (Q) of the flip-flop follows the data input (D) while the clock input (C) is high. Latching occurs when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$).
(Note: Clock (C) Overrides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to three-state, non-inverting output buffers. These buffers have a common control line (EN); enabling the buffer to transmit the data from the outputs of the data latch (Q) or disabling the buffer, forcing the output into a high impedance state (three-state).

This high-impedance state allows the designer to connect the μPB8212 directly to the microprocessor bi-directional data bus.

Control Logic

The μPB8212 has four control inputs: $\overline{DS}_1$, DS_2, MD and STB. These inputs are employed to control device selection, data latching, output buffer state and the service request flip-flop.

$\overline{DS}_1$, DS_2 (Device Select)

These two inputs are employed for device selection. When $\overline{DS}_1$ is low and DS_2 is high ($\overline{DS}_1 \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

Service Request Flip-Flop (SR)

The (SR) flip-flop is employed to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output (Q) of the (SR) flip-flop is connected to an inverting input of a "NOR" gate. The other input of the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS}_1 \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

MD (Mode)

This input is employed to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is in the output mode (high) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS}_1 \cdot DS_2$).

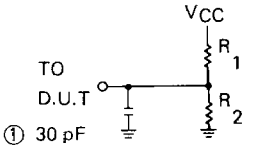
When MD is in the input mode (low) the output buffer state is determined by the device selection logic ($\overline{DS}_1 \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

STB is employed as the clock (C) to the data latch for the input mode (MD = 0) and to synchronously reset the service request flip-flop (SR).

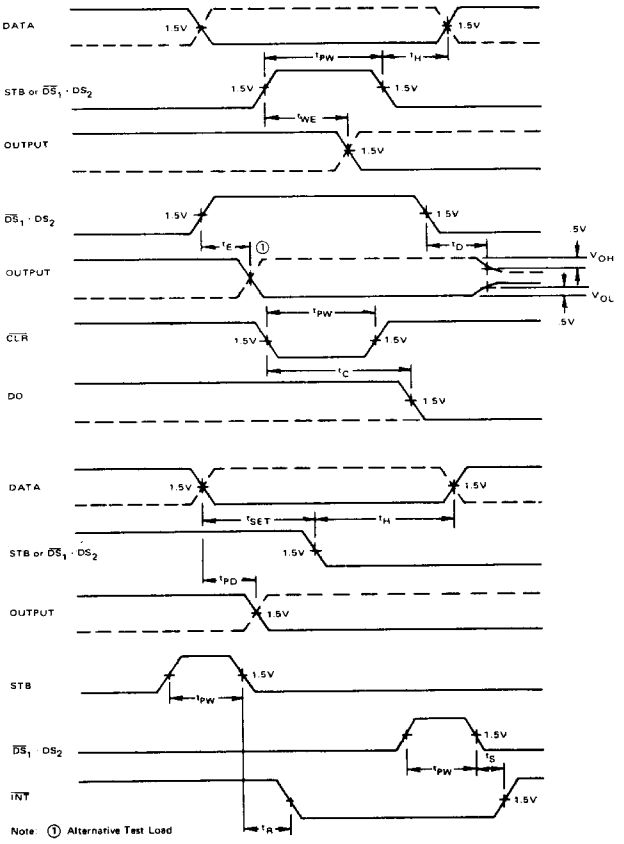
Note that the SR flip-flop triggers on the negative edge of STB which overrides $\overline{CLR}$.

TIMING WAVEFORMS



Note: ① Including Jig and Probe Capacitance

TEST CIRCUIT



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Package Outlines

For information, see Package Outline Section 7.

Plastic, μPB8212C
Cerdip, μPB8212D